FLUKE®

Variable clock architecture for ARBs avoids the limitations of DDS

Application Note

The 284 Waveform Genereator is a 4-channel 100 MHz variable clock arbitrary waveform generator with multiple bus interfaces and waveform storage.

Recently, function generators based on direct digital synthesis (DDS) have been developed into arbitrary/function generators with impressive specifications. However, the DDS approach to arbitrary waveform generation imposes serious limitations which are not immediately obvious. The alternative approach of a variable clock architecture offers a greater level of flexibility and can be used to solve many more real-world problems.

Most digital waveform generators use waveform data stored in RAM. As the RAM address is incremented, the values are output sequentially to a Digital-to-Analog-Converter (DAC). The DAC reconstructs the waveform as a series of voltage steps, which are subsequently filtered before being passed to the output amplifier and attenuators. The frequency of the output waveform is determined by the rate at which the RAM addresses are changed.

In the first arbitrary generators, the RAM address was incremented by a simple counter. The waveform's rate of replay was set by varying the clock frequency into the counter. The system was later refined so that individual sections of the RAM could be addressed and clocked at will. However, the basic principle of accessing successive RAM locations at a rate defined by a variable frequency clock remained. This is referred to as variable clock architecture.

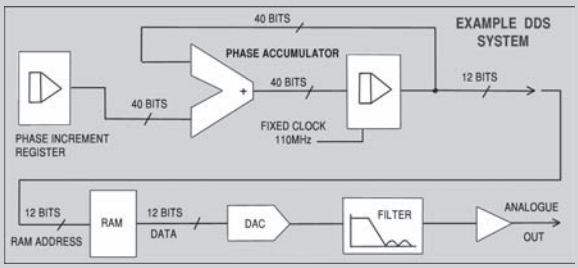
More recently, direct digital synthesis (DDS), a technique originally designed for generating variable frequency sine waves, has become the most widely used technique for arbitrary waveform generation.

This article explores the relative strengths and weaknesses of the DDS and variable clock architectures for arbitrary waveform generation.

Direct digital synthesis

Most digital function generators use a direct digital synthesis (DDS) system. In a DDS generator, the RAM address increment rate is determined from a fixed clock frequency by a digital block comprising a phase increment register and a phase accumulator.

The RAM is loaded with the amplitude values of the individual points of one cycle (360 degrees) of the desired waveform (e.g. a sinusoid). Typically, the number of points used will be made equal to or greater than the number of vertical amplitude points.



Example: For a 12-bit system with a 4096 word waveform store, an Fmax. of 40 MHz and a frequency resolution of 0.0001 Hz.

One complete cycle of the selected waveform is stored in RAM as 4096 12-bit amplitude values. As the RAM address is incremented, the waveform values are output sequentially to the DAC, which reconstructs the waveform as a series of voltage steps. Sinewaves and triangles are subsequently filtered to smooth the steps in the DAC output.

The frequency of the output waveform is determined by the rate at which the RAM addresses are changed; in a DDS system the address changes are generated as follows.

The RAM contains the amplitude values of all the individual points of 1 cycle (360°) of the waveform; each sequential address change corresponds to a phase increment of the waveform of 360°/4096. Instead of using a counter to generate sequential RAM addresses, a phase accumulator is used to increment the phase.

On each clock cycle the phase increment, which has been loaded into the phase increment register by the CPU, is added to the current result in the phase accumulator; the 12 most significant bits of the phase accumulator drive the RAM address lines. The output waveform frequency is now determined by the size of the phase increment at each clock. If each increment is the same size then the output frequency is constant; if it changes, the output frequency changes but with phase continuity.

The example uses a 40-bit accumulator and a clock frequency which is $2^{40} \times 10^{-4}$ (~109.951 MHz); this yields a frequency resolution (corresponding to the smallest phase increment) of $fCLK/2^{40} = 0{\cdot}1$ mHz.

Only the 12 most significant bits of the phase accumulator are used to address the RAM. At a waveform frequency of fCLK/4096 (~27 kHz), the RAM address increments on every clock. At all frequencies below this (i.e. at smaller phase increments), one or more addresses are output for more than one clock period, because the phase increment is not big enough to step the address at every clock. Similarly, at waveform frequencies above 27 kHz, the larger phase increment causes some addresses to be skipped, giving the effect of the stored waveform being 'sampled'; different points will be sampled on successive cycles of the waveform.

The minimum number of points required to reproduce a waveshape accurately will determine the maximum useful output frequency: fmax = fCLK/No. of points. For sinewaves, a suitably designed filter permits the waveform to be reproduced accurately towards the Nyquist limit (fCLK/2), although because of practical limitations to the filter performance, a lower limit may be set (e.g. 40 MHz for a 110 MHz clock). For other waveforms, the required number of points depends upon the complexity of the waveform and the precision with which it must be reproduced.

Waveform jitter

The DDS principle is particularly well suited to generating sinusoidal waveforms. The output filter can create a low distortion sinusoid from a very small number of points per cycle, approaching the Nyquist limit of two. For non-sinusoidal waveforms such as pulses, triangles and ramps, sharp transitions are included, which can not be passed through an output filter unless the repetition rate is low. Hence, for a 100 MHz clock generator, sinewaves may be available up to 40 MHz or more, but triangles and ramps may be limited to 500 kHz or less. This is true for all types of arbitrary generator.

An arbitrary waveform might consist only of a combination of sinusoids (e.g. a harmonic distortion waveform), but many will contain spikes, edges and other rapid transitions. This is where the limitations of the DDS type of arbitrary generator start to show.

The DDS arbitrary generator only faithfully reproduces an arbitrary waveform at a repetition rate equal to the DDS clock frequency divided by the waveform length (or sub-multiples of this). At all other frequencies, samples are either omitted or are duplicated an uneven number of times. For repetitive waveforms this results in waveform jitter, because the starting address will change when the addressing wraps around to the beginning of the memory. At high repetition rates the waveform will be "sampled," which may lead to parts of the waveform being skipped over.

Note that the jitter effects are a function of the master clock period and will become relatively insignificant at low waveform repetition rates.

By contrast, the variable clock system replays the waveform exactly as it was defined. Every waveform point is replayed in sequence with the rate of replay being set by the clock frequency.

External clock synchronization

Variable clock arbitrary generators have the potential for the waveform to be clocked in direct synchronism with an external signal by using it as the waveform clock.

It is a common requirement to generate arbitrary waveform in direct synchronism with some external signal which varies in frequency.

DDS generators operate with a fixed waveform clock frequency. This can be phase locked to a fixed frequency external signal, but can not replicate the external ARB clock capability of the variable clock generator.

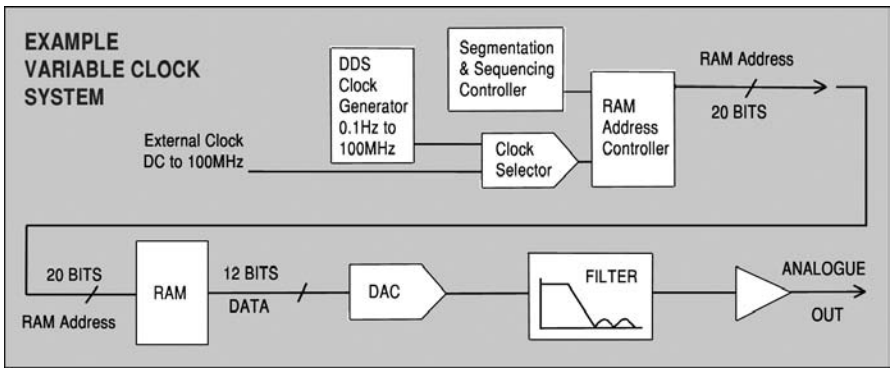
Waveform complexity

The DDS type of arbitrary generator imposes restrictions on the waveform length. Unlike a variable-clock generator, the number of samples replayed must be equal to a fixed length (normally a power of two). Undesirable interpolation or extrapolation of the original waveform may be needed to achieve this.

The amount of memory needed to reproduce a complex waveform accurately may be quite large. The amount provided on a particular generator may vary from one thousand words up to one million words or more.

Waveform memory is expensive, as it has to be constructed from high speed static RAMs. Consequently, lower cost arbitrary generators provide limited waveform memory. In a DDS system, the whole of the arbitrary waveform must be contained within the memory length, which may limit the complexity of the waveforms that can be generated.

Variable clock generators, however, can incorporate sophisticated address selection hardware that allows them to access specific sections of the waveform memory and therefore perform complex sequencing.

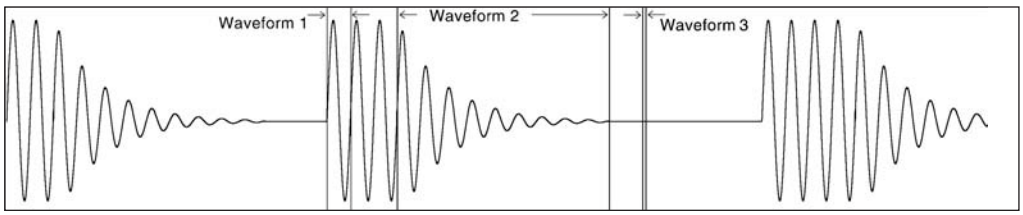


Many real-world waveforms include repetitive elements. By using a segment of the memory to recreate each repeating element, the waveform can be constructed from a "sequence" in which the individual elements are replayed in a defined order and with a defined number of repetitions (loop count). In this way waveforms can be created with a much greater number of points than the waveform memory size.

Sequencing and looping also provide a convenient facility for modifying an arbitrary waveform without the need to recreate it.

For example, a waveform might consist of a series of complex events separated by periods of inactivity. By creating each null period from a loop count of a short null waveform, the time between each event can be changed, simply by changing each loop count value.

Alternatively, the delay between events may need to be responsive to external signals. The sequence can be arranged such that the change from one waveform segment to the next is initiated by an external trigger signal.



Simple waveform sequence

In this example the requirement is for three sinewave bursts, each of a different length, followed by an exponential decay. The delay between bursts is also unequal.

By using sequencing, the complete arbitrary waveform can be constructed simply and quickly from three basic arbitrary waveforms—a single cycle sinewave (W1), a decaying sinewave (W2), and a short dc level (W3). These base waveforms might well be taken from the user's library of useful waveshapes.

A nine step sequence is constructed of the form:

W1x N1 > W2 > W3 x D1 > W1 x N2 > W2 > W3 x D2 > W1 x N3 > W2 > W3 x D3.

N and D are loop counts for the sequence (i.e. the number of times that the waveform is repeated before the sequence steps on). N defines the sine burst count while D defines the delay. By making the dc level (W 3) very short, the delay time can be defined to a high accuracy.

Changes to the waveform, such as variations in the delays, can now be managed with ease (changing a loop count can be done by simply selecting the value and rotating the spin wheel).

On a DDS-based arbitrary generator, it would be necessary to construct the complete waveform using a waveform construction program on a PC. Even the smallest change would require the complete waveform to be regenerated and downloaded again.

Mixed technology generators

Despite its disadvantages for complex arbitrary waveform generation, DDS remains a powerful technique that offers particular advantages for the generation of high speed repetitive waveforms.

If a waveform is constructed from 500 waveform points, the maximum waveform repetition rate for a 100 MHz variable clock generator is 200 kHz unless the waveform is redefined within a smaller number of points. The DDS generator, however, effectively reduces the waveform length automatically as the frequency increases by virtue of its sampling technique.

This can be particularly useful where a waveform needs to be swept over a wide frequency range. The DDS generator can provide full waveform resolution at low frequencies while retaining the ability to sweep up to high frequencies (though at the expense of waveform precision).

Some waveform generators incorporate both a variable-clock architecture and a DDS architecture within the same unit, to offer the widest possible range of capabilities. The Fluke 280 and 290 series are examples of this type of arbitrary waveform generator.

Multiple channels

Many situations require multiple arbitrary waveforms to be generated simultaneously. Most single channel generators, both variable-clock and DDS, provide the facility to phase lock to another generator in order to achieve this. Where multiple outputs are regularly needed however, a dedicated multi-channel generator will be required.

Variable clock architecture provides considerably greater flexibility for generating complex and precise inter-channel relationships than does DDS.

The Fluke 284 (40 MS/S) and 294 (100 MS/s), for example, offer four channels, which can be either fully independent or linked to provide inter-channel triggering, modulation, summing and phase control. Any number of channels can also be simultaneously clocked by an external signal. This gives the ability to generate dynamic, real time complex signals as part of a larger test system. The 294 adds the flexibility of CompactFlash waveform storage.

Waveform creation

Many generators include some level of built-in waveform editing, such as point-by-point value insertion, straight line interpolation and standard waveform insertion between points.

However, complex arbitrary waveforms can only be created outside of the generator using PC based waveform creation/editing software.

For this purpose Fluke provides Waveform Manager Plus software, operating under Windows. Waveform Manager Plus incorporates comprehensive facilities for waveform creation and editing, incorporating standard waveform libraries, freehand drawing, and a sophisticated mathematical equation editor, and the ability to paste data directly from Microsoft™ Excel.

The need to use external waveform creation software can be a serious disadvantage if the generator is being used in a stand-alone environment. However, the sequencing capability of a variable clock generator means that new waveforms may be created and existing ones modified by simply changing the sequencing parameters. For maximum flexibility, it is useful to keep a library of waveform elements within the generator. With this in mind, Fluke has equipped the 290 series generators with removable CompactFlash based waveform storage. Up to 500 waveforms can be stored on a single card, and large project specific waveform libraries could be maintained using multiple cards.

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